Remarks

Reconsideration of the present application is respectfully requested in view of the foregoing amendments and following remarks. Claims 1-22 and 24-36 are pending in the application. Claims 1, 32, 35, and 36 are independent. Claims 1-3, 5, 7, 8, 20, 30-32, 35, and 36 have been amended. Claim 23 has been canceled. No claims have been allowed. Claims 1-22 and 24-36 have been rejected. These rejections are respectfully traversed.

Patentability of Claims 1-5, 7, 9-14, 18, 20, 21, 24, 30, and 31 over Madden in view of Paterson and Ravichandran under 35 U.S.C. § 103(a)

Claims 1-5 and 7, 9-14, 18, 20, 21, 24, 30 and 31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,119,483 to Madden et al. ("Madden") in view of U.S. Patent No. 6,983,237 to Paterson et al. ("Paterson") and in further view of U.S. Patent No. 5,966,537 to Ravichandran ("Ravichandran"). These rejections are respectfully traversed.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2142.)

Motivations to combine or modify references must come from the references themselves or be within the body of knowledge in the art. (MPEP § 2143.01.)

Independent claim 1 is directed to a method, and recites:

> simulating a first hardware component in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment;
> simulating a second hardware component in the circuit design with a second simulation

model in the EDA environment;

identifying state information comprising a transfer from the first simulation model in the EDA simulation environment, said transfer being directed to the second simulation model;

receiving the state information from the first simulation model; and

making the state information available to the second simulation model without simulating the transfer in the circuit design (emphasis added).

In its rejection of independent claim 1, the Action relies on Madden. Madden is understood as describing a system that uses an instruction decoder segment and a first execution segment of a pipelined processor, where the two segments have registers or queues ("state silos") "that are operative during normal instruction execution to save a sufficient amount of state information to immediately restart the instruction decoder segment and the first execution segment by reloading the state information having been stored in the state silos" (*see* Abstract). Neither the cited section nor any other section of Madden, however, is understood to teach or suggest simulating a first hardware component in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second hardware component in the circuit design with a second simulation model in the EDA environment, let alone identifying state information comprising a transfer from the first simulation model in the EDA simulation environment, said transfer being directed to the second simulation model, as recited in independent claim 1.

In its rejection of independent claim 1, the Action also relies on various passages in Paterson, but Applicants respectfully submit that Paterson does not cure the deficiencies of Madden. For example, Paterson describes "a computer-based simulation model" that "commences with the performance of a first simulation operation" and has a second simulation operation that "commences with a configuration captured from a preceding simulation operation" (*see* Abstract, as noted in the Action). Accordingly, Paterson is understood to describe multiple simulation operations performed with a single simulation model. Applicants respectfully submit, however, that neither the cited section

nor any other section of Paterson is understood to teach or suggest simulating a first hardware component in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second hardware component in the circuit design with a second simulation model in the EDA environment, let alone identifying state information comprising a transfer from the first simulation model in the EDA simulation environment, said transfer being directed to the second simulation model, as recited in independent claim 1.

In its rejection of independent claim 1, the Action also relies on various passages in Ravichandran, but Applicants respectfully submit that Ravichandran does not cure the deficiencies of Madden or Paterson. For example, the Action cites Ravichandran at col. 6, lines 39-41: "The simulation indicates which instructions will not be executed and the frequency at which the instructions are executed given the particular input data." Applicants respectfully submit, however, that neither the cited section nor any other section of Ravichandran is understood to teach or suggest simulating a first hardware component in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second hardware component in the circuit design with a second simulation model in the EDA environment, let alone identifying state information comprising a transfer from the first simulation model in the EDA simulation environment, said transfer being directed to the second simulation model, as recited in independent claim 1.

Therefore, Applicants respectfully submit that Madden, Paterson, and Ravichandran, individually or in combination with one another, do not teach or suggest all of the claim limitations of independent claim 1 as required to establish a prima facie case of obviousness. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of independent claim 1 be withdrawn.

Dependent claims 2-5 and 7, 9-14, 18, 20, 21, 24, 30 and 31 depend directly or indirectly from

independent claim 1 and are allowable for at least the reasons recited above with respect to their parent claim 1. Moreover, claims 2-5 and 7, 9-14, 18, 20, 21, 24, 30 and 31 recite combinations of features that are independently patentable. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejections of dependent claims 2-5 and 7, 9-14, 18, 20, 21, 24, 30 and 31 be withdrawn.

Patentability of Claims 6, 8-10, 12, 14-16, 18-22, 24-29, and 31 over Madden in view of Paterson, Ravichandran, and Bailey under 35 U.S.C. § 103(a)

Claims 6, 8-10, 12, 14-16, 18-22, 24-29, 31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,119,483 to Madden et al. ("Madden") in view of U.S. Patent No. 6,983,237 to Paterson et al. ("Paterson") and U.S. Patent No. 5,966,537 to Ravichandran ("Ravichandran") and in further view of Bailey et al., "Hardware/Software Co-Simulation Strategies for the Future" ("Bailey"). These rejections are respectfully traversed.

Dependent claims 6, 8-10, 12, 14-16, 18-22, 24-29, 31 depend directly or indirectly from independent claim 1 and are allowable for at least the reasons recited above with respect to their parent claim 1. Moreover, claims 6, 8-10, 12, 14-16, 18-22, 24-29, 31 recite combinations of features that are independently patentable. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejections of dependent claims 6, 8-10, 12, 14-16, 18-22, 24-29, 31 be withdrawn.

Patentability of Claims 32-36 over Madden in view of Paterson and Bailey under 35 U.S.C. § 103(a)

Claims 32-36 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,119,483 to Madden et al. ("Madden") in view of U.S. Patent No. 6,983,237 to Paterson et al. ("Paterson") and in further view of Bailey et al., "Hardware/Software Co-Simulation Strategies for

the Future" ("Bailey"). These rejections are respectfully traversed.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2142.)

Motivations to combine or modify references must come from the references themselves or be within the body of knowledge in the art. (MPEP § 2143.01.)

Claims 32-34

Independent claim 32 is directed to a method, and recites:

> simulating a first abstraction level of a circuit functionality in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment;
> simulating a second abstraction level of the circuit functionality in the circuit design with a second simulation model in the EDA environment;
> reading state information from the first simulation model in the EDA simulation environment when a simulation domain of the first simulation model is deactivated; and
> writing the state information to the second simulation model in the EDA simulation environment prior to activation of a simulation domain of the second simulation model (emphasis added).

In its rejection of independent claim 32, the Action relies on Madden. Madden is understood as describing a system that uses an instruction decoder segment and a first execution segment of a pipelined processor, where the two segments have registers or queues ("state silos") "that are operative during normal instruction execution to save a sufficient amount of state information to immediately restart the instruction decoder segment and the first execution segment by reloading the state information having been stored in the state silos" (*see* Abstract). Neither the cited section nor any other section of Madden, however, is understood to teach or suggest simulating a first abstraction level

of a circuit functionality in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second abstraction level of the circuit functionality in the circuit design with a second simulation model in the EDA environment, let alone reading state information from the first simulation model in the EDA simulation environment when a simulation domain of the first simulation model is deactivated or writing the state information to the second simulation model in the EDA simulation environment prior to activation of a simulation domain of the second simulation model, as recited in independent claim 32.

In its rejection of independent claim 32, the Action also relies on various passages in Paterson, but Applicants respectfully submit that Paterson does not cure the deficiencies of Madden. For example, Paterson describes "a computer-based simulation model" that "commences with the performance of a first simulation operation" and has a second simulation operation that "commences with a configuration captured from a preceding simulation operation" (*see* Abstract, as noted in the Action). Accordingly, Paterson is understood to describe multiple simulation operations performed with a single simulation model. Applicants respectfully submit, however, that neither the cited section nor any other section of Paterson is understood to teach or suggest simulating a first abstraction level of a circuit functionality in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second abstraction level of the circuit functionality in the circuit design with a second simulation model in the EDA environment, let alone reading state information from the first simulation model in the EDA simulation environment when a simulation domain of the first simulation model is deactivated or writing the state information to the second simulation model in the EDA simulation environment prior to activation of a simulation domain of the second simulation model, as recited in independent claim 32.

In its rejection of independent claim 32, the Action also relies on various passages in

Ravichandran, but Applicants respectfully submit that Ravichandran does not cure the deficiencies of Madden or Paterson. For example, the Action cites Ravichandran at col. 6, lines 39-41: "The simulation indicates which instructions will not be executed and the frequency at which the instructions are executed given the particular input data." Applicants respectfully submit, however, that neither the cited section nor any other section of Ravichandran is understood to teach or suggest simulating a first abstraction level of a circuit functionality in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second abstraction level of the circuit functionality in the circuit design with a second simulation model in the EDA environment, let alone reading state information from the first simulation model in the EDA simulation environment when a simulation domain of the first simulation model is deactivated or writing the state information to the second simulation model in the EDA simulation environment prior to activation of a simulation domain of the second simulation model, as recited in independent claim 32.

Therefore, Applicants respectfully submit that Madden, Paterson, and Ravichandran, individually or in combination with one another, do not teach or suggest all of the claim limitations of independent claim 32 as required to establish a prima facie case of obviousness. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of independent claim 32 be withdrawn.

Dependent claims 33 and 34 depend directly or indirectly from independent claim 32 and are allowable for at least the reasons recited above with respect to their parent claim 32. Moreover, claims 33 and 34 recite combinations of features that are independently patentable. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejections of dependent claims 33 and 34 be withdrawn.

Claim 35

Independent claim 35 is directed to a machine readable medium having stored thereon machine executable instructions that when executed implement a method comprising:

> simulating a first hardware component in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment;
> simulating a second hardware component in the circuit design with a second simulation model in the EDA environment;
> identifying state information comprising a transfer from the first simulation model in the EDA simulation environment, said transfer being directed to the second simulation model;
> receiving the state information from the first simulation model; and
> making the state information available to the second simulation model without simulating the transfer in the circuit design (emphasis added).

In its rejection of independent claim 35, the Action relies on Madden. Madden is understood as describing a system that uses an instruction decoder segment and a first execution segment of a pipelined processor, where the two segments have registers or queues ("state silos") "that are operative during normal instruction execution to save a sufficient amount of state information to immediately restart the instruction decoder segment and the first execution segment by reloading the state information having been stored in the state silos" (*see* Abstract). Neither the cited section nor any other section of Madden, however, is understood to teach or suggest simulating a first hardware component in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second hardware component in the circuit design with a second simulation model in the EDA environment, let alone identifying state information comprising a transfer from the first simulation model in the EDA simulation environment, said transfer being directed to the second simulation model, as recited in independent claim 35.

In its rejection of independent claim 35, the Action also relies on various passages in Paterson, but Applicants respectfully submit that Paterson does not cure the deficiencies of Madden. For

example, Paterson describes "a computer-based simulation model" that "commences with the performance of a first simulation operation" and has a second simulation operation that "commences with a configuration captured from a preceding simulation operation" (*see* Abstract, as noted in the Action). Accordingly, Paterson is understood to describe multiple simulation operations performed with a single simulation model. Applicants respectfully submit, however, that neither the cited section nor any other section of Paterson is understood to teach or suggest simulating a first hardware component in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second hardware component in the circuit design with a second simulation model in the EDA environment, let alone identifying state information comprising a transfer from the first simulation model in the EDA simulation environment, said transfer being directed to the second simulation model, as recited in independent claim 35.

In its rejection of independent claim 35, the Action also relies on various passages in Ravichandran, but Applicants respectfully submit that Ravichandran does not cure the deficiencies of Madden or Paterson. For example, the Action cites Ravichandran at col. 6, lines 39-41: "The simulation indicates which instructions will not be executed and the frequency at which the instructions are executed given the particular input data." Applicants respectfully submit, however, that neither the cited section nor any other section of Ravichandran is understood to teach or suggest simulating a first hardware component in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second hardware component in the circuit design with a second simulation model in the EDA environment, let alone identifying state information comprising a transfer from the first simulation model in the EDA simulation environment, said transfer being directed to the second simulation model, as recited in independent claim 35.

Therefore, Applicants respectfully submit that Madden, Paterson, and Ravichandran,

individually or in combination with one another, do not teach or suggest all of the claim limitations of independent claim 35 as required to establish a prima facie case of obviousness. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of independent claim 35 be withdrawn.

Claim 36

Independent claim 36 is directed to a machine readable medium having stored thereon machine executable instructions that when executed implement a method comprising:

> simulating a first abstraction level of a circuit functionality in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment;
> simulating a second abstraction level of the circuit functionality in the circuit design with a second simulation model in the EDA environment;
> reading state information from the first simulation model in the EDA simulation environment when a simulation domain of the first simulation model is deactivated; and
> writing the state information to the second simulation model in the EDA simulation environment prior to activation of a simulation domain of the second simulation model (emphasis added).

In its rejection of independent claim 36, the Action relies on Madden. Madden is understood as describing a system that uses an instruction decoder segment and a first execution segment of a pipelined processor, where the two segments have registers or queues ("state silos") "that are operative during normal instruction execution to save a sufficient amount of state information to immediately restart the instruction decoder segment and the first execution segment by reloading the state information having been stored in the state silos" (*see* Abstract). Neither the cited section nor any other section of Madden, however, is understood to teach or suggest simulating a first abstraction level of a circuit functionality in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second abstraction level of the circuit functionality in the circuit design with a second simulation model in the EDA environment, let alone

reading state information from the first simulation model in the EDA simulation environment when a simulation domain of the first simulation model is deactivated or writing the state information to the second simulation model in the EDA simulation environment prior to activation of a simulation domain of the second simulation model, as recited in independent claim 36.

In its rejection of independent claim 36, the Action also relies on various passages in Paterson, but Applicants respectfully submit that Paterson does not cure the deficiencies of Madden. For example, Paterson describes "a computer-based simulation model" that "commences with the performance of a first simulation operation" and has a second simulation operation that "commences with a configuration captured from a preceding simulation operation" (*see* Abstract, as noted in the Action). Accordingly, Paterson is understood to describe multiple simulation operations performed with a single simulation model. Applicants respectfully submit, however, that neither the cited section nor any other section of Paterson is understood to teach or suggest simulating a first abstraction level of a circuit functionality in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second abstraction level of the circuit functionality in the circuit design with a second simulation model in the EDA environment, let alone reading state information from the first simulation model in the EDA simulation environment when a simulation domain of the first simulation model is deactivated or writing the state information to the second simulation model in the EDA simulation environment prior to activation of a simulation domain of the second simulation model, as recited in independent claim 36.

In its rejection of independent claim 36, the Action also relies on various passages in Ravichandran, but Applicants respectfully submit that Ravichandran does not cure the deficiencies of Madden or Paterson. For example, the Action cites Ravichandran at col. 6, lines 39-41: "The simulation indicates which instructions will not be executed and the frequency at which the

instructions are executed given the particular input data." Applicants respectfully submit, however, that neither the cited section nor any other section of Ravichandran is understood to teach or suggest simulating a first abstraction level of a circuit functionality in a circuit design with a first simulation model in an electronic design automation (EDA) simulation environment or simulating a second abstraction level of the circuit functionality in the circuit design with a second simulation model in the EDA environment, let alone reading state information from the first simulation model in the EDA simulation environment when a simulation domain of the first simulation model is deactivated or writing the state information to the second simulation model in the EDA simulation environment prior to activation of a simulation domain of the second simulation model, as recited in independent claim 36.

Therefore, Applicants respectfully submit that Madden, Paterson, and Ravichandran, individually or in combination with one another, do not teach or suggest all of the claim limitations of independent claim 36 as required to establish a prima facie case of obviousness. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of independent claim 36 be withdrawn.

Request for Interview

If any issues remain, the Examiner is formally requested to contact the undersigned attorney prior to issuance of the next Office Action in order to arrange a telephonic interview. It is believed that a brief discussion of the merits of the present application may expedite prosecution. Applicants submit the foregoing formal Amendment so that the Examiner may fully evaluate Applicants' position, thereby enabling the interview to be more focused.

This request is being submitted under MPEP § 713.01, which indicates that an interview may be arranged in advance by a written request.

Conclusion

The claims in their present form should now be allowable. Such action is respectfully requested.

Respectfully submitted,

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